a charge pump, coupled between said DSP and said DAA, said charge pump providing operating power to said DAA, said charge pump doubling the voltage of said clock signal.

2. An interface circuit as set forth in claim 1, wherein said charge pump comprises:

a1 cont.

a first capacitive element having an input side connected to said DSP and an output side connected to said DAA;

a second capacitive element having an input and an output each connected to said DAA; and

a rectifying element coupled between the output side of said first capacitive element and said second capacitive element, said rectifying element receiving said clock signal from said DSP and doubling the voltage of said clock signal before passing said clock signal to said DAA.

7. A method of providing power to a data access arrangement (DAA) in an interface circuit of a telecommunication network when a telephone line connected to said interface circuit is in the on-hook state, said interface circuit including a digital signal processor (DSP) having a clock generator, said method comprising the steps of:

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inserting a charge pump between said DSP and said DAA;

generating a power signal, having a voltage, across said charge pump by inputting the output of said clock generator to said charge pump; and

doubling the voltage of said power signal and storing said generated power signal for use by said interface.

8. An interface circuit, comprising:

a driver circuit for developing a charge across capacitive elements of said interface circuit, said charge having a voltage;

a data access arrangement (DAA); and

a charge pump, coupled between said DAA and said driver circuit, said charge pump providing operating power to said DAA, said charge pump doubling the voltage of said charge and passing said doubled voltage to said DAA to provide said operating power.

9. An interface circuit as set forth in claim 8, wherein said charge pump comprises:

a first capacitive element having an input side connected to said driver circuit and an output side connected to said DAA;

a second capacitive element having an input and an output each connected to said DAA; and

a rectifying element coupled between the output side of said first capacitive element and said second capacitive element, said rectifying element receiving said charge from said driver circuit and doubling the voltage of said charge before passing said charge to said DAA.

Add the following claims.

--14. An interface circuit as set forth in claim 1, wherein said interface circuit is a fully differential circuit.

~~15. An interface circuit as set forth in claim 2, wherein said first capacitive~~

element has:

a maximum capacitance of 500 pF; and

a minimum capacitance of 10 pF.

16. An interface circuit as set forth in claim 2, wherein the first capacitive element has a capacitance value of approximately 100 pF.

17. An interface circuit as set forth in claim 8, wherein said interface circuit is a fully differential circuit.

18. An interface circuit as set forth in claim 9, wherein said first capacitive element has:

a maximum capacitance of 500 pF; and

a minimum capacitance of 10 pF.

19. An interface circuit as set forth in claim 9, wherein the first capacitive element has a capacitance value of approximately 100 pF.--

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In the Drawings

On page 2 of the Office Action, the Examiner indicated that drawings filed on November 16, 1998 are acceptable for examination purposes only. On June 9, 1999, formal drawings were filed which are believed to overcome any objections made due to informalities. It is respectfully submitted that the formal drawings filed on June 9, 1999 comply fully with the drawing requirements.